

### FEATURES

#### Dual output

RFOUT = 11.4 GHz to 12.8 GHz

RFOUT/2 = 5.7 GHz to 6.4 GHz

Very wide tuning range: VTUNE = 2 V to 18 V

#### High output power

RFOUT = 12 dBm

RFOUT/2 = 4 dBm

Low phase noise: -111 dBc/Hz @ 100 kHz offset

Current consumption: 310 mA typical

Small package: 32-lead 5 mm × 5 mm LFCSP

Flexible bias control allows either 5 V or 3 V operation

### APPLICATIONS

Point-to-point radios

VSAT radios

Communications test equipment

### GENERAL DESCRIPTION

The [ADF5582](#) is a GaAs monolithic microwave integrated circuit (MMIC) voltage-controlled oscillator (VCO), packaged in an industry standard 32-lead 5 mm × 5 mm LFCSP package. The [ADF5582](#) utilizes a push-push VCO architecture and outputs both the fundamental and half frequency output. The VCO's phase noise performance of -115 dBc/Hz at 100 kHz

offset allow it to meet the requirements of demanding radio systems like microwave point-to-point links. The divide-by-2 output can be input directly into Analog Devices, Inc., PLLs such as the [ADF4156](#), [ADF4106](#), or [ADF4150HV](#). The [ADF5582](#) operates off a 5 V supply and outputs 15 dBm typical.

### FUNCTIONAL BLOCK DIAGRAM

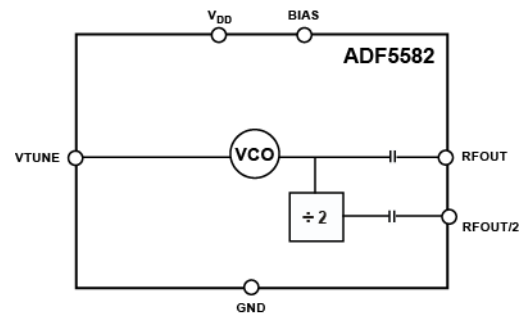


Figure 1.

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**REVISION HISTORY**

## SPECIFICATIONS

VDD = 5 V  $\pm$  10%, 3 V  $\pm$  5%, GND = 0 V; dBm referred to 50  $\Omega$ ; T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. The operating temperature range is -40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>RF CHARACTERISTICS</b>					
Output Frequency: RFOUT	11.4		12.8	GHz	
Divide-by-2 Output Frequency: RFOUT/2	5.7		6.4	GHz	
<b>5 V Operation</b>					
Output Power: RFOUT	TBD	+12		dBm	
Output Power: RFOUT/2	TBD	+4		dBm	
Single Side Band Phase Noise		-111		dBc/Hz	VTUNE = 5 V, offset = 100 kHz
Single Side Band Phase Noise		-133		dBc/Hz	VTUNE = 5 V, offset = 1 MHz
<b>3 V Operation</b>					
Output Power: RFOUT	TBD	TBD		dBm	
Output Power: RFOUT/2	TBD	TBD		dBm	
Single Side Band Phase Noise		TBD		dBc/Hz	VTUNE = 5 V, offset = 100 kHz
Single Side Band Phase Noise		TBD		dBc/Hz	VTUNE = 5 V, offset = 1 MHz
Tune Voltage	2		18	V	
Tuning Port Leakage			TBD	$\mu$ A	VTUNE = 18 V
VCO Pushing		TBD		MHz/V	VTUNE = 5 V
VCO Pulling		TBD		MHz/pp	Into a 2:1 voltage standing wave ratio (VSWR)
Frequency Drift Rate			TBD	MHz/°C	
Output Return Loss		TBD		dB	
<b>HARMONICS</b>					
Subharmonic at RFOUT/2		-TBD		dBc	On the RFOUT pin
Second Harmonic Content		-TBD		dBc	
Third Harmonic Content		-TBD		dBc	
<b>POWER SUPPLIES</b>					
<b>IDD</b>					
5 V		310	TBD	mA	T <sub>A</sub> = 25°C
3 V		TBD	TBD	mA	T <sub>A</sub> = 25°C

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VDD to GND	-0.3 V to +5.5 V
VTUNE	25 V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
LFCSP $\theta_{JA}$ Thermal Impedance <sup>1</sup> (Paddle Soldered)	40.11°C/W
Peak Temperature	260°C
Time at Peak Temperature	40 sec

<sup>1</sup> Two signal planes (that is, on top and bottom surfaces of the board), two buried planes and nine vias.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

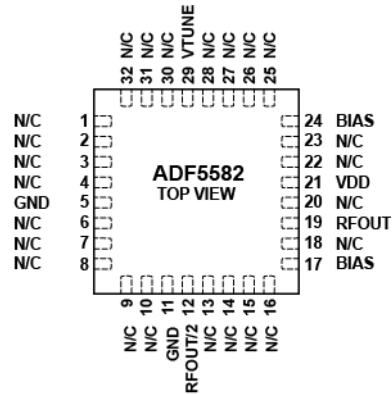
This device is a high performance RF integrated circuit and is ESD sensitive. Proper precautions should be taken for handling and assembly.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NC = NO CONNECT  
THE EXPOSED PADDLE MUST BE  
CONNECTED TO GND

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
5, 11	GND	RF Ground. Tie all ground pins together.
12	RFOUT/2	Half-Frequency Output.
17, 24	BIAS	VCO Bias. Both pins should be connected together, see Figure 3 and Figure 4 for bias network.
19	RFOUT	Fundamental Frequency Output.
21	VDD	Voltage Supply for the VCO. Decouple this pin to ground with 120 pF, 1 nF, and 1 μF capacitors.
29	VTUNE	Tuning Port for the VCO.
1 to 4, 6 to 10, 13 to 16, 18, 20, 22, 23, 25 to 28, 30 to 32	NC	These pins are not connected internally (see Figure 2).
33	EP	Exposed Pad. The LFCSP package has an exposed pad that must be connected to GND.

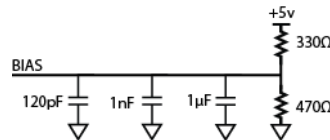


Figure 3. Bias Network for 5 V Operation

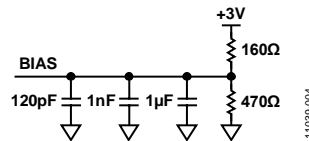


Figure 4. Bias Network for 3 V Operation

TYPICAL PERFORMANCE CHARACTERISTICS

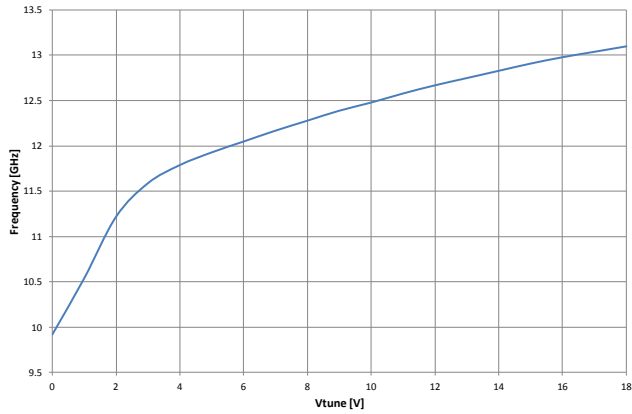


Figure 5. Frequency vs. Tuning Voltage

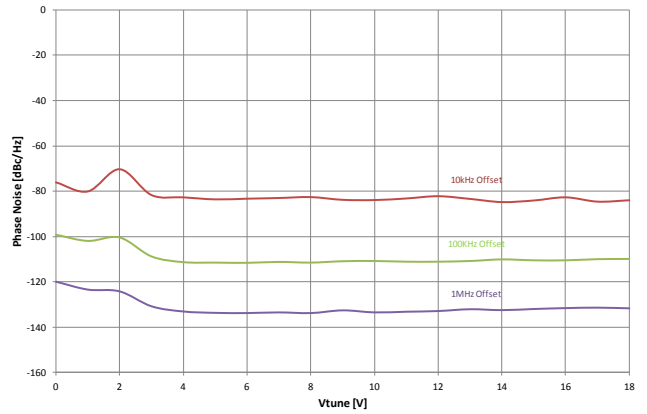


Figure 8. Phase Noise vs. Tuning Voltage

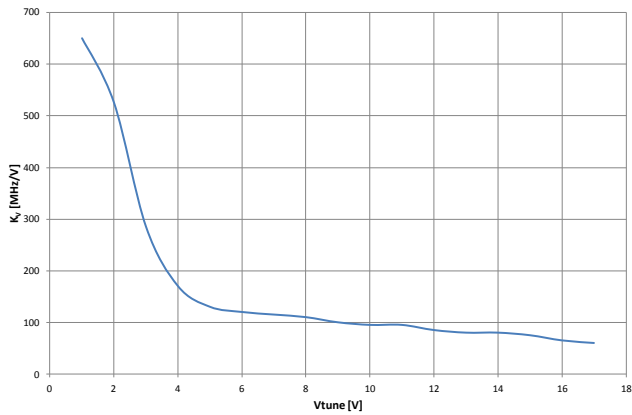


Figure 6. Sensitivity vs. Tuning Voltage

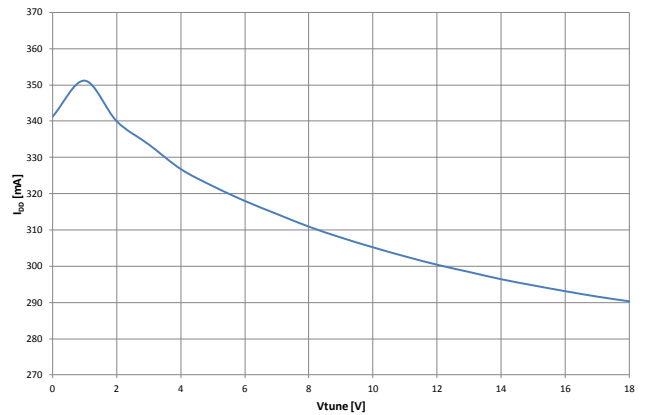


Figure 9. IDD vs. Tuning Voltage

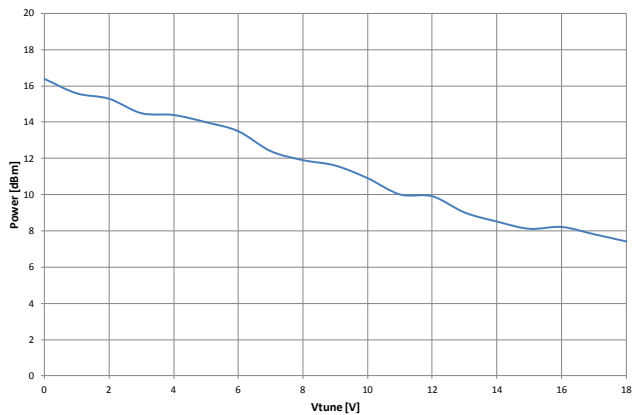


Figure 7. Output Power vs. Tuning Voltage

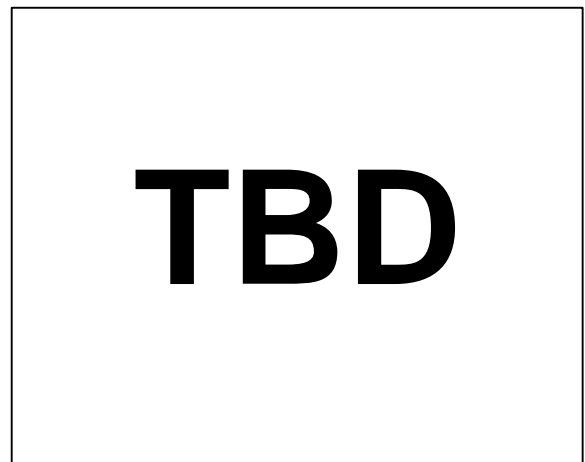


Figure 10. Phase Noise vs. Temperature

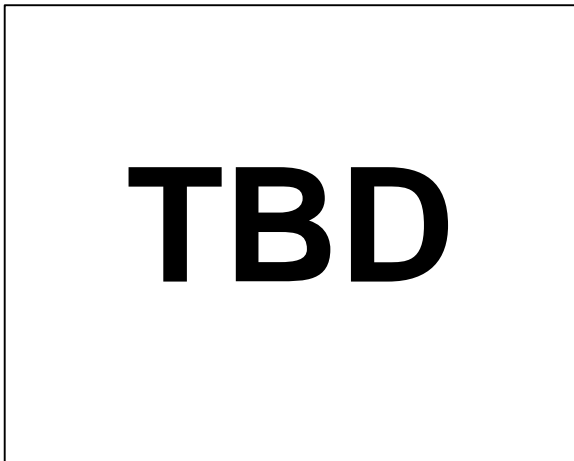


Figure 11. RFOUT/2 Frequency vs. Tuning Voltage

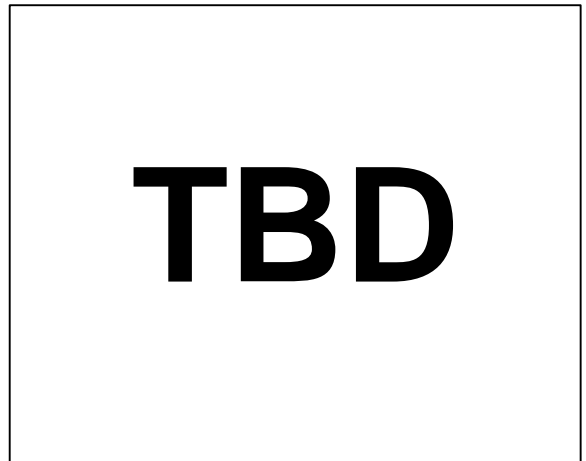


Figure 14. Phase Noise vs. VBIAS with VTUNE = 6V

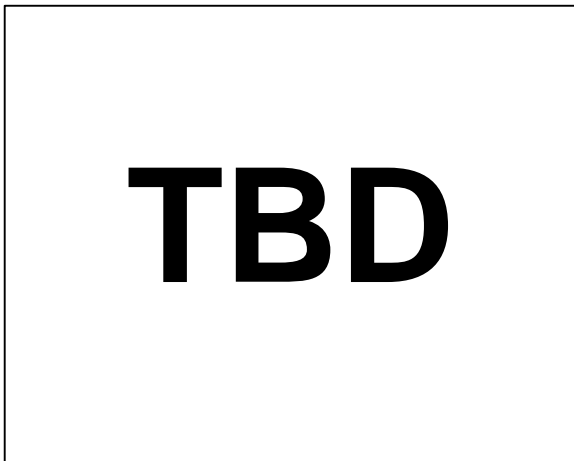


Figure 12. RFOUT/2 Output Power vs. Tuning Voltage

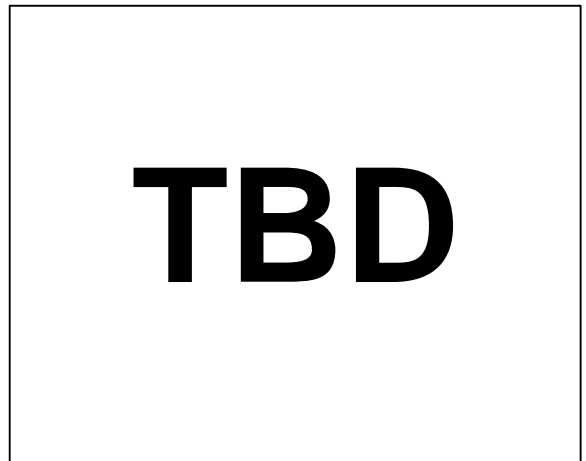


Figure 15. Output Power vs. VBIAS with VTUNE = 6V

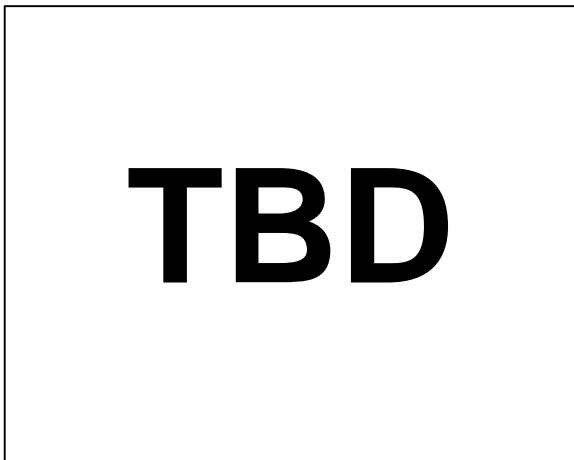


Figure 13. RFOUT/2 Phase Noise vs. Tuning Voltage

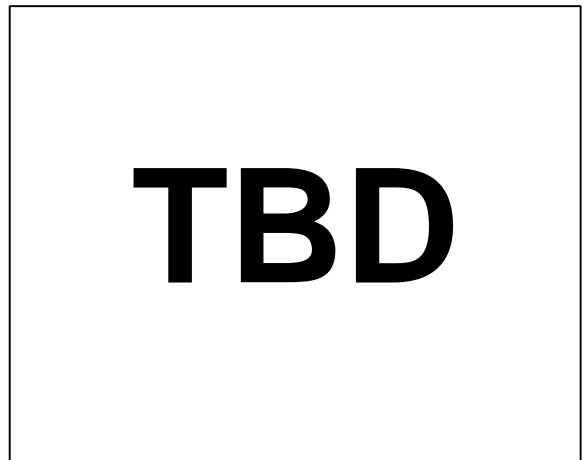


Figure 16. IDD vs. VBIAS with VTUNE = 6V

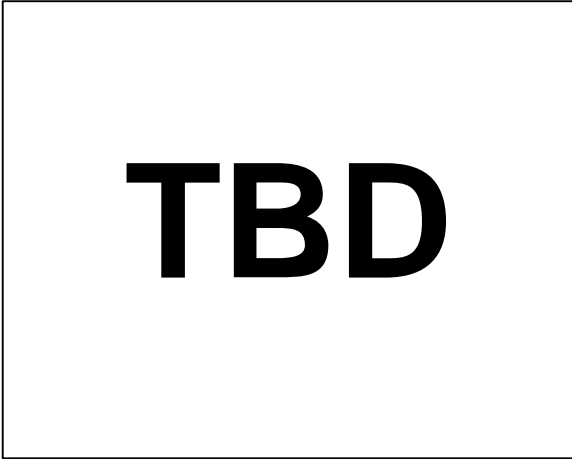


Figure 17. Frequency vs. Tuning Voltage with VDD = 3V

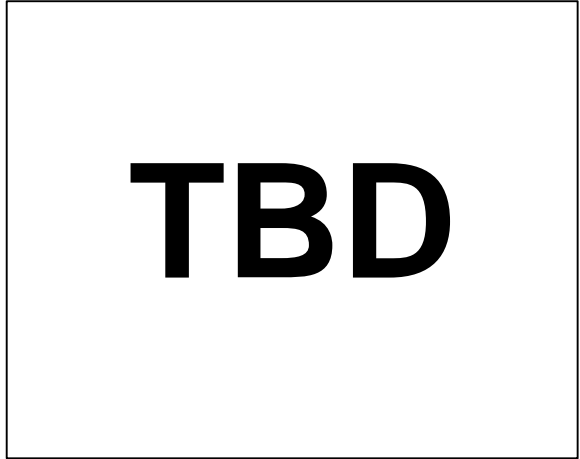


Figure 20. Phase Noise vs. Tuning Voltage with VDD = 3V

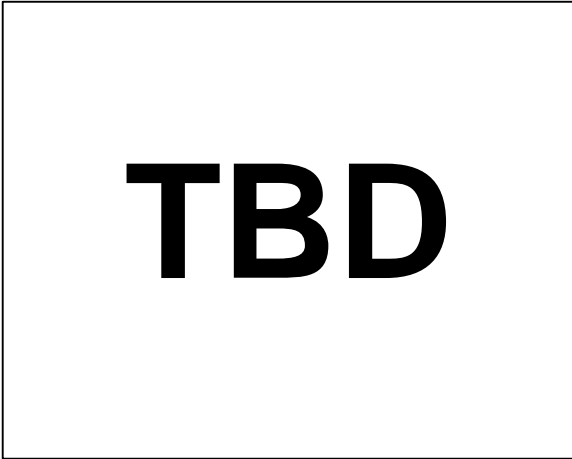


Figure 18. Sensitivity vs. Tuning Voltage with VDD = 3V

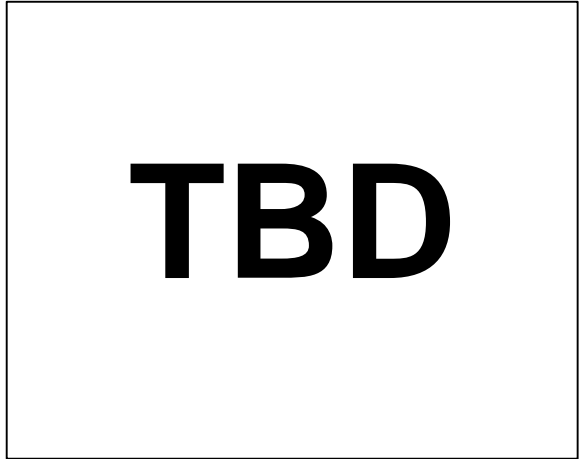


Figure 21. IDD vs. Tuning Voltage with VDD = 3V

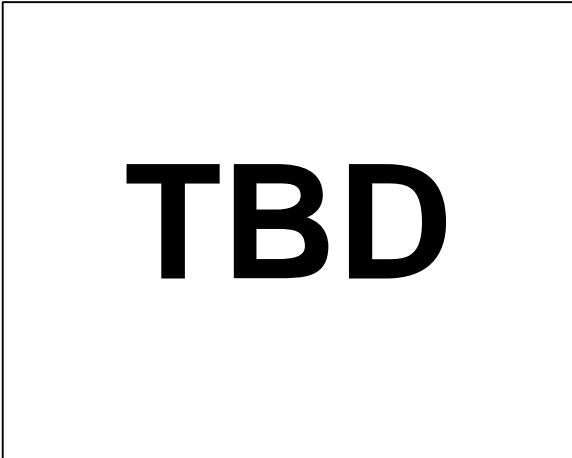


Figure 19. Output Power vs. Tuning Voltage with VDD = 3V



## APPLICATION CIRCUIT

The [ADF5582](#) can be operated in a PLL loop with several of the Analog Devices PLL family of ICs by using the divide-by-2 output from the VCO.

A simple interface is shown in Figure 22 using the [ADF4108](#) high frequency PLL to drive the [ADF5582](#). An active filter topology, using the [OP184](#) op amp, can be used to provide the wide tuning range required by the [ADF5582](#). The positive input pin of the [OP184](#) is biased at half the [ADF4108](#) charge pump supply ( $V_P$ ). This can be easily achieved using a simple resistor

divider, ensuring sufficient decoupling close to the +IN A pin of the [OP184](#), thereby allowing the use of a single positive supply for the op amp.

To achieve the best performance of the [ADF5582](#), take care in the power management design. On the [ADF5582](#) evaluation board, the [ADP7104](#) low noise LDO is used to provide the 5 V power supply to the part and provide the voltage for the resistor divider network for the BIAS pin.

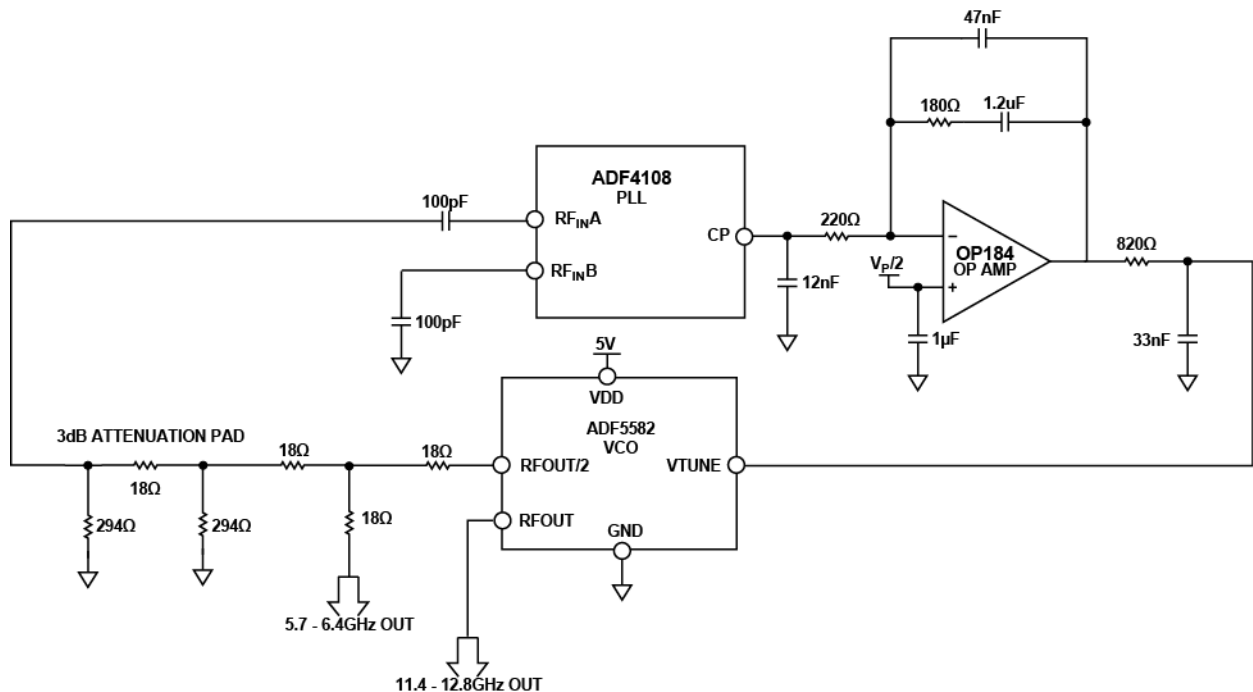
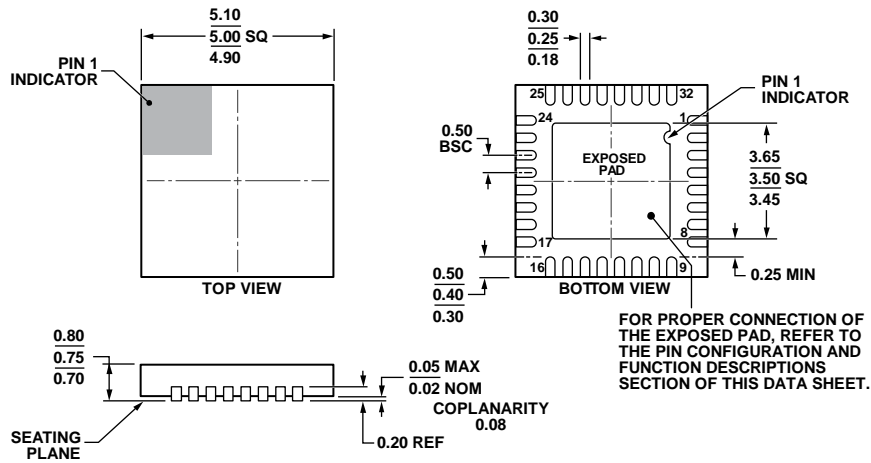


Figure 22. [ADF5582](#) used with [ADF4108](#) in a Microwave 12.0 GHz PLL Loop

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 23. 32-Lead Lead Frame Chip Scale Package [LF CSP\_WQ]  
 5 mm × 5 mm Body, Very Thin Quad  
 (CP-32-13)  
 Dimensions shown in millimeters

112408-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADF5582BCPZ-U3	-40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LF CSP_WQ)	CP-32-13
EV-ADF5582EB2Z-U3		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

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